INSTITUT "JOŽEF STEFAN"
RAČUNALNIŠKI SISTEMI
Kompetenčni center CLEC

tetramax

System design on FPGAs

On-line Workshop

20. Oct. 2021, 12:30-16:00

This course provides an introduction to system design on FPGA devices using prototype boards (Zedboard, Zybo, …) and Vivado design software suite. The participants will learn to design HDL system, to design an embedded system targeting ARM processor of Zynq FPGA device using Vivado and IP Integrator, to create custom peripherals and to add them to the design system, to write an embedded software application and to debug it, and to debug HDL design. In the end, some advanced topics of system design on FPGA like High-Level Synthesis (HLS) and dynamic partial reconfiguration will be introduced.

The lecturer is an assistant prof. dr. Anton Biasizzo from the Computer systems department at Jožef Stefan Institute.

Participation is free! All welcome!

Applications are accepted until 18. 10. 2021. More information: Kompetenčni center CLEC (clec@ijs.si).

Register now!

Course program:

- Fundamentals of FPGA structure and Vivado design flow
- HDL design flow and design constraints
- Embedded system design flow
- IP design and integration
- Software application development
- System debugging using a logic analyzer
- Advanced topics (HLS, reconfiguration)

Prerequisites:
Knowledge of the VHDL language, the basic knowledge of designing with FPGAs, and a basic understanding of C programming language is recommended for the participants.

Note: The language at the workshop will be Slovene or English, at the choice of the participants.

SRIPTOP Strateško razvojno inovacijsko partnerstvo TOVARNE PRIHODNOSTI
SRIP PMiS
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